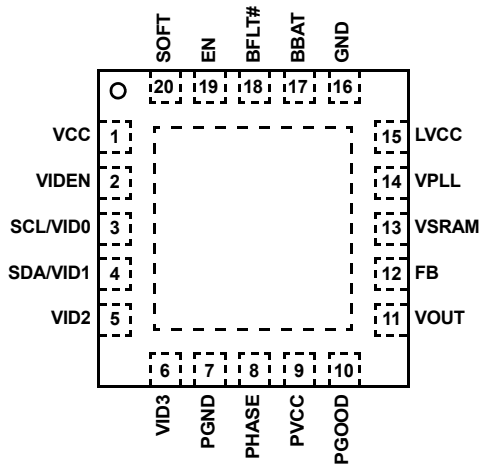
Integrated XScale Regulator

The ISL6271A is a versatile power management IC (PMIC) designed for the Xscale type of processors. The device integrates three regulators, two fault indicators and an I^2C bus for communication with a host microprocessor. Two of the three regulators function as low power, low drop out regulators, designed to power SRAM and phase-lock loop circuitry internal to the Xscale processor. The third regulator uses a proprietary switch-mode topology to power the processor core and facilitate Dynamic Voltage Management (DVM), as defined by Intel.

Since power dissipation inside a microprocessor is proportional to the square of the core voltage, Intel XScale processors implement DVM as a means to more efficiently utilize battery capacity. To support this power saving architecture, the ISL6271A integrates an I^2C bus for communication with the host processor. The processor, acting as the bus master, transmits a “voltage level” and “voltage slew rate” to the ISL6271A appropriate to the processing requirements; higher core voltages support higher operating frequencies and code execution. The bus is fully compliant with the Phillips® I^2C protocol and supports both standard and fast data transmission modes. Alternatively, the output of the core regulator can be programmed in 50mV increments from 0.85V to 1.6V using the input Voltage ID (VID) pins. All three regulators share a common enable pin and are protected against overcurrent, over temperature and undervoltage conditions. When disabled via the enable pin, the ISL6271A enters a low power state that can be used to conserve battery life while maintaining the last programmed VID code and slew rate. An integrated soft-start circuit transitions the ISL6271A output voltages to their default values at a rate determined by an external soft-start capacitor.

Pinout

ISL6271A (4x4 QFN) TOP VIEW



Features

- Three Voltage Regulators (1 Buck, 2 LDOs)
- High-Efficiency, fully-Integrated synchronous buck regulator with DVM
- 800mA DC output current for the buck regulator
- Proprietary ‘Synthetic Ripple’ Control Topology
- Greater than 1MHz Switching Frequency
- Diode emulation for light load efficiency
- I^2C Interface Module for DVM from 0.85V to 1.6V
- Optional fixed 4-bit VID-control in lieu of DVM
- Small Output Inductor and Capacitor
- Battery Fault signal
- Input Supply Voltage Range: 2.76V-5.5V
- 4x4 mm QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-free Available (RoHS Compliant)

Applications

- PDA
- Cell Phone
- Tablet Devices
- Embedded Processors

Related Literature

- Technical Brief TB379 “*Thermal Characterization of Packaged Semiconductor Devices”*
- Technical Brief TB389 “*PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages“*
- Application Note AN1139 *“Setup Instruction for the ISL6271 Evaluation Kit”*

Ordering Information

PART NUMBER*	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6271ACR	-25 to 85	20 Ld 4x4 QFN	L20.4x4
ISL6271ACRZ (Note)	-25 to 85	20 Ld 4x4 QFN (Pb-free)	L20.4x4

*Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Absolute Maximum Ratings

(PVCC, VCC, LVCC) to GND 7V
PHASE to PGND . . . . . .-0.3V to (PVCC +0.3V)
PGND to GND . . . . . -0.3V to 0.3V
All other pins to GND . . . . . .-0.3V to 7V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package (Notes 1, 2)	45	7.5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Recommended Operating Conditions

Ambient Temperature Range . . . . . .-25°C to 85°C
Supply Voltage (PVCC, VCC) . . . . . 2.76 to 5.5V
Supply Voltage (LVCC) . . . . . 1.7 - 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features (TB379).
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications — Operating Conditions, Unless Otherwise Noted; T_A = -25°C to 85°C, PVCC = VCC = 3.7V. Component values as shown in Figure 19, Typical Application Circuit: Vout = 1.6V, I_{OUT} = 0mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CORE BUCK REGULATOR						
Input Voltage Range (After V_{CC} reaches Rising V_{POR})	PV_{CC}	$PV_{CC} = V_{CC}$	2.76		5.5	V
Output Voltage Nominal Range	VOUT	Programmable in 50mV increments	0.85		1.60	V
Max. DC Output Current	Icore	(Note 3)	800			mA
Current Limit (DC plus Ripple)	Icore_lim	(wafer level test only)	950	1300		mA
PMOS on Resistance	$r_{DS(ON)p}$	Iout = 200mA		275		mΩ
NMOS on Resistance	$r_{DS(ON)n}$	Iout = 200mA		140		mΩ
Frequency (Note 4)	f	Vin = 3.7V, Vo = 1.0V, VF6 = 0.9V		1.2		MHz
Load Regulation		VOUT = 1.6V; Io = 1mA-500mA		.05	1	%
Line Regulation		Over VCC range		1		%
VOUT Pk-Pk Ripple	V_{P-P}	Vout = 1.6V, I = 0.4A, CCM		5		mV
		Discontinous Mode Operation		10		mV
System Accuracy		Over Temperature	-1		2	%
		Room Temperature	-1		1	%
Under Voltage Threshold (Note 5)		Rising, as % of nominal VOUT		94		%
		Falling, as % of nominal VOUT		86		%
Over Voltage threshold		Rising, as % of nominal VOUT		114		%
		Falling, as % of nominal VOUT		106		%
Start-up Time	t_{st}	From Enable Active @ Io = 10mA; Vo = 1.6V		1.3		ms
Ring Damping Switch Resistance	$R_{on(RD)}$			50	75	Ω
LINEAR REGULATORS						
Input Voltage	LVCC	Connected to PVCC	2.76		5.5	V
		Not connected to PVCC	1.70		3.5	V
Output Voltage	VSRAM			1.1		V
	VPLL			1.3		V

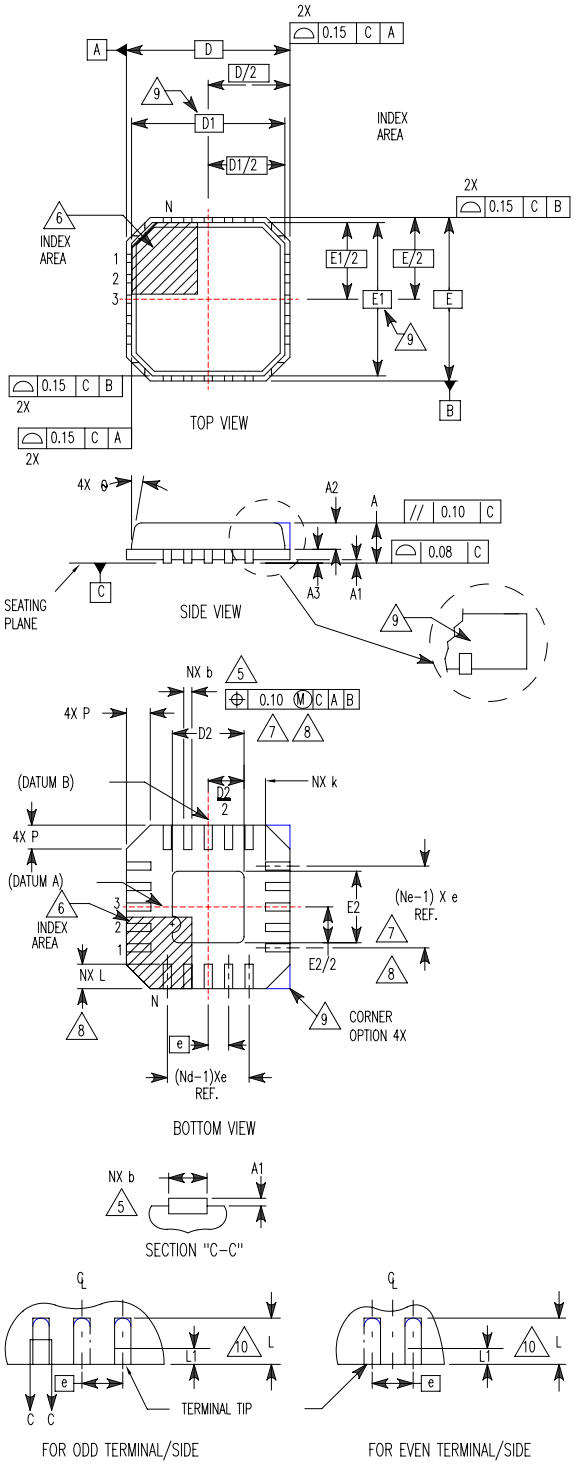
Electrical Specifications Operating Conditions, Unless Otherwise Noted; T_A = -25°C to 85°C, PVCC = VCC = 3.7V. Component values as shown in Figure 19, Typical Application Circuit: Vout = 1.6V, I_{OUT} = 0mA **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Tolerance		Iout = 1mA	-2.5		2.5	%
Maximum Average Output Current	I_SRAM		50			mA
	I_PLL		40			mA
Current Limit	I_{ldo_lim}	Each LDO regulator	120	300		% (Note 7)
Line Regulation		LVCC = 1.7-5.5V			0.25	%
Load Regulation		Io = 1 to 25mA			.5	%
Undervoltage Threshold		Rising - % of VPLL, VSRAM		91		%
		Falling - % of VPLL, VSRAM		86		%
Start-Up Time	tst	Soft-start power up to 1.3V, Csoft = 10nF		1.3		ms
SYSTEM						
Supply Current (VCC)	I_Q	I_{core} = No load		380		µA
	I_Q	EN = 0V		2	5	µA
Supply Current (LVCC)	I_{LVCC}			25		µA
EN Voltage	V_{IH}		2.0			V
	V_{IL}				0.55	V
Soft-Start Source Current (Controlled by I^2C control bits D5, D4)	I_{00}		3.4	4.8	6.2	µA
	I_{01}		6.7	9.6	12.5	µA
	I_{10}		16	24	32	µA
	I_{11}		30	47	64	µA
Temperature Shutdown	T_r	Rising T	130	140	150	°C
	T_f	Falling T	85	95	105	°C
POR/BFLT# Threshold (Note 6)	V_{POR}	Rising VCC	2.60	2.80	3.0	V
	V_{POR}	Falling VCC	2.44	2.60	2.76	V
PGOOD Pull Down Resistance	R_{on}			700	960	Ω
VIDEN, VID2, VID3 Voltage Threshold	$V_{IH(VID)}$		2.4			V
	$V_{IL(VID)}$				1.0	V
I^2C LOGIC						
SCL, SDA Voltage Threshold	$V_{IH(I^2C)}$		2.0			V
	$V_{IL(I^2C)}$				0.55	V
SDA Pull Down Resistance	$R_{on(SDA)}$				132	Ω

NOTES:

3. Guaranteed by design; correlated with statistic data for PVCC = VCC from 3.5V to 5.5V.
4. Switching frequency is a function of input, output voltage and load.
5. As a result of an over-current condition exceeding 800mA. Will result in a PGOOD fault.
6. A high rising POR tracks with a high falling POR.
7. Percentage of Maximum Average Output Current (I_SRAM or I_PLL).

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.4x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VGGD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne	5	5		3
P	-	-	0.60	9
θ	-	-	12	9

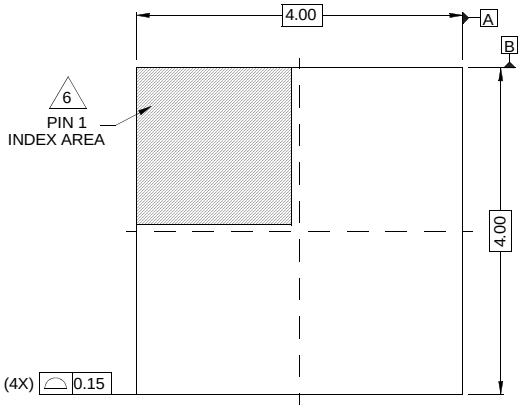
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

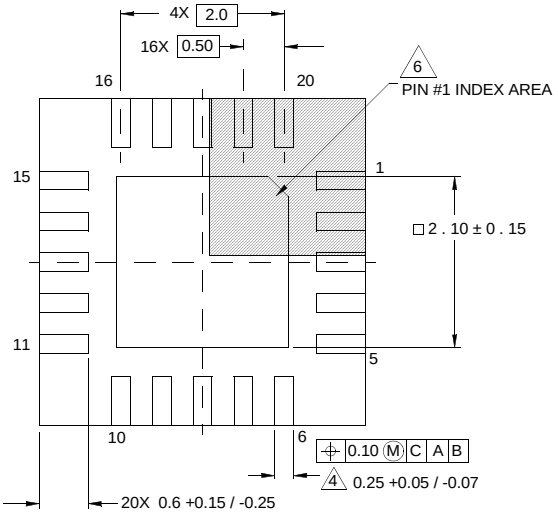
Package Outline Drawing

L20.4x4

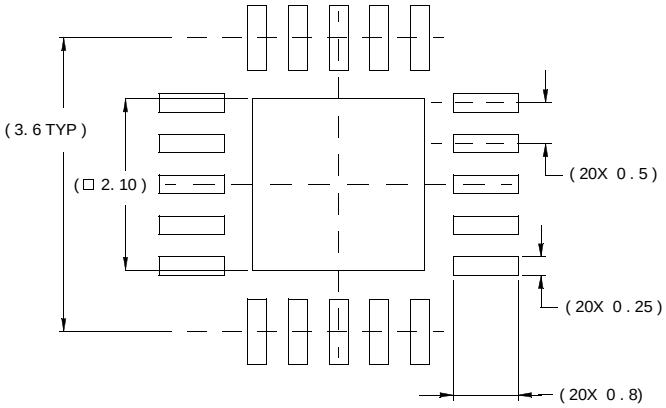
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE



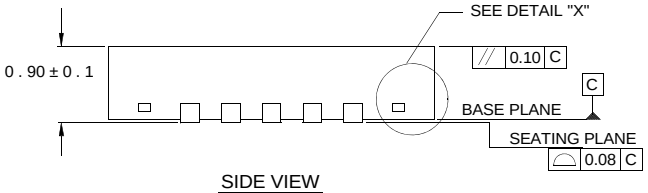
TOP VIEW



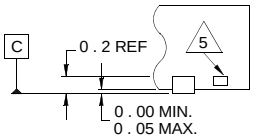
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.